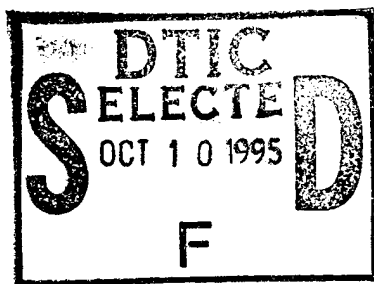


**Complementary 2-D MESFET for
Low Power Electronics**



Interim Report # 6

**Air Force SBIR Phase I
Contract Number: F33615-95-C-1679**

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**Complementary 2-D MESFET for Low Power Electronics
(AirForce SBIR Contract F33615-95-C-1679)**

Phase I Interim Report #6

As detailed in the Phase I proposal, the project has four major tasks. These are 1) assessment of the p-channel 2-D MESFET device fabrication, 2) development of a p-channel 2-D MESFET model and implementation of the model into AIM-SPICE, 3) circuit simulations of complementary 2-D MESFET circuits using AIM-SPICE and comparison with conventional circuits, and, 4) analysis of manufacturability and technology insertion issues. This report summarizes progress in each task area through 28 SEP 95.

Task 1: Assessment of p-Channel Device Fabrication

The assessment of the p-channel 2-D MESFET device fabrication is underway. A heterostructure wafer was obtained from an MBE vendor and device fabrication is now getting under way using an ADT maskset used previously for n-channel devices. A second wafer has been obtained from Vitesse Semiconductor Corporation and will be used for diagnostic purposes (contacts to p-type GaAs). Device data will be presented in the next report.

Task 2: Development of p-Channel 2-D MESFET Model

The p-channel 2-D MESFET model has been implemented into AIM-Spice for simulation of p-channel 2-D MESFET *I-V* characteristics as well as complementary 2-D MESFET logic circuits (see previous reports). Once device data is available, the model parameters will be updated to better predict p-channel characteristics.

Task 3: Complementary 2-D MESFET Circuit Simulations

Preliminary circuit simulations of complementary 2-D MESFET circuits have been performed (see last report) and more extensive simulations will be conducted using the model revised as per the data to be obtained in the coming weeks.

Task 4: Manufacturability and Technology Insertion Issues

This task will be summarized in the Final Report.

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